INTEGRATED PACKET BIT ERROR RATE TESTER FOR 10G SERDES

ABSTRACT OF THE DISCLOSURE

An integrated packet bit error rate tester includes a packet transmit circuit that has a first memory for storing transmit packet data and is connectable to a channel under test. A packet receive circuit includes a second memory for storing received packet data and is connectable to the channel under test. An interface is used for programming the packet transmit and packet receive circuits. The packet transmit circuit can generate an arbitrary 10G SERDES packet in response to commands from the interface. The packet receive circuit can determine a bit error rate of the channel under test. The second memory can capture received packet data upon any one of (a) after a pre-programmed pattern is detected, (b) after a pre-programmed pattern is lost, and (c) after an error is detected.

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